AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A variable gain amplifier, comprising:

a voltage-current converter for converting voltages of a wide input range into currents;

a current shared circuit for receiving the currents from the voltage-current converter and controlling output currents values depending on first and second control voltages; and

a current-voltage converter for converting the output currents from the current shared circuit into differential voltages depending on a bias voltage in order to obtain a variable gain;

wherein the voltage-current converter further comprises:

a first NMOS transistor connected ~~to~~ between a power supply terminal and a first output terminal and driven by a first input voltage; and

a second NMOS transistor connected ~~to~~ between the power supply terminal and a second output terminal and driven by a second input voltage.

2. (Cancelled)

3. (Currently Amended) The variable gain amplifier as claimed in claim 1, wherein the voltage-current converter further comprises:

~~the first NMOS transistor connected between the power supply terminal and a first output terminal and driven by a first input voltage;~~

~~the second NMOS transistor connected between the power supply terminal and a second output terminal and driven by a second input voltage;~~

a first current source connected between the first output terminal and a ground terminal; and

a second current source connected between a second output terminal and the ground terminal.

4. (Original) The variable gain amplifier as claimed in claim 1, wherein the current shared circuit comprises:

a first NMOS transistor connected between a first input terminal and a first output terminal and driven by the first control voltage;

a second NMOS transistor connected between a second input terminal and a second output terminal and driven by the first control voltage;

a third NMOS transistor connected between the first input terminal and the second output and driven by the second control voltage; and

a fourth NMOS transistor connected between the second input terminal and the first output terminal and driven by the second control voltage, wherein the output currents are controlled by adjusting transconducances of the first to fourth NMOS transistors.

5. (Original) The variable gain amplifier as claimed in claim 1, wherein the current-voltage converter comprises:

a first NMOS transistor connected between a first input terminal and a first output terminal and driven by the bias voltage;

a second NMOS transistor connected between a second input terminal and a second output terminal and driven by the bias voltage;

first and second current sources each connected between the first input terminal and the second output terminal, and a ground terminal; and

first and second resistors each connected between the first and second output terminals, and the power supply terminal.

6. (Original) The variable gain amplifier as claimed in claim 1, wherein the current-voltage converter comprises:

a first NMOS transistor connected between a first input terminal and a first output terminal and driven by a first bias voltage;

a second NMOS transistor connected between a second input terminal and a second output terminal and driven by the first bias voltage;

a third NMOS transistor connected between the first input terminal and a ground terminal and driven by a second bias voltage;

a fourth NMOS transistor connected between the second input terminal and the ground terminal and driven by the second bias voltage; and

first and second load means each connected between the first and second output terminals, and the power supply terminal.

7. (Original) The variable gain amplifier as claimed in claim 6, wherein each of the first and second load means is a resistor.

8. (Previously Presented) The variable gain amplifier as claimed in claim 6, wherein each of the first and second load means comprises:

a PMOS transistor connected between the power supply terminal and the output terminal and driven by the potential of a first node;

a NMOS transistor connected between the output terminal and the first node and driven by the potential of the output terminal; and

a capacitor and a current source connected in parallel between the first node and the ground terminal.